DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 08/24/2009 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 43, 48-53, 89 and 94-99 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,495,442 to Lin et al (Lin) in view of U.S. Pat. No. 6,528,380 to Woolery et al. (Woolery).

Re claim 43: Lin discloses a chip structure comprising:

a silicon substrate (10, col 4 line 49);

a resistor in said silicon substrate (not shown but “transistors and other devices” is described in col 4 lines 49-51),

a MOS device (not shown but described as “transistors and other devices” in col 4 lines 49-51) comprising a portion in said silicon substrate;

a metallization structure (14) over said silicon substrate, wherein said metallization structure comprises a first metal layer (interconnect portion 13 of first layer of 14) and a second metal layer (interconnect portion 13 of second layer of 14) over said first metal layer;

a first dielectric (white portion of layer 14) layer between said first and second metal layers;

a passivation layer (18, col 5 lines 4-5) over the metallization structure and over said dielectric layer, wherein a first opening in said passivation layer is over a first contact point (16; col 4 lines 57-67) of said metallization structure and said first contact point is at a bottom of said first opening, and a second opening (16) in said passivation layer is over a second contact point of said metallization structure and said second contact point is at a bottom of said second opening, wherein a gap (created by passivation layer 18) is between said first and second contact points, wherein said passivation layer comprises an insulating nitride layer (col 5 lines 4-5); and

a circuit trace (26/22/36/28/38) over the passivation layer and on said first and second contact points (16), wherein said first contact point is connected to said second contact point through said circuit trace (38/28/38 connect first and second points 16), and wherein said circuit trace is connected to said resistor (col 4 lines 66-67, col 5 line 1-2 describe point of contact 16 as connected to the transistors and other devices on the surface of substrate 10, which would include the resistor. col 5 lines describe

contact point 16 also in electrical contact with 22/36/38, which is the circuit trace. Thus the resistor on surface of substrate is connected to the circuit trace through contact 16) through said first opening (16).

Lin fails to disclose the resistor in said silicon substrate comprises silicon with a dopant. Woolery teaches a chip structure (Figures 4A-4J) with a silicon substrate (400) and a resistor ("Resistor") in said silicon substrate, where said resistor comprises silicon with a dopant (arsenic, col 9 lines 53-56). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lin to have a resistor in the silicon substrate where said resistor comprises silicon with a dopant as in Woolrey in order to be able to predetermine and set the device resistivity.

Re claim 89: Lin discloses a chip structure comprising:

a silicon substrate (10, col 4 line 49);

a resistor in said silicon substrate (not shown but "transistors and other devices" is described in col 4 lines 49-51),

a MOS device (not shown but described as "transistors and other devices" in col 4 lines 49-51) comprising a portion in said silicon substrate;

a metallization structure (14) over said silicon substrate, wherein said metallization structure comprises a first metal layer (interconnect portion 13 of first layer of 14) and a second metal layer (interconnect portion 13 of second layer of 14) over said first metal layer;

a dielectric (white portion of layer 14) layer between said first and second metal layers;

a passivation layer (18, col 5 lines 4-5) over the metallization structure and over said dielectric layer; wherein a first opening in said passivation layer is over a first contact point (16; col 4 lines 57-67) of said metallization structure and said first contact point is at a bottom of said first opening, and wherein a second opening (16) in said passivation layer is over a second contact point of said metallization structure and said second contact point is at a bottom of said second opening, wherein a gap (created by passivation layer 18) is between said first and second contact points, wherein said passivation layer comprises an insulating nitride layer (col 5 lines 4-5)

a circuit trace (26/22/36/28/38) over the passivation layer and on said first and second contact points (16), wherein said first contact point is connected to said second contact point through said circuit trace (38/28/38 connect first and second points 16),, wherein said circuit trace is connected to said resistor (col 4 lines 66-67, col 5 line 1-2 describe point of contact 16 as connected to the transistors and other devices on the surface of substrate 10, which would include the resistor. col 5 lines describe contact point 16 also in electrical contact with 22/36/38, which is the circuit trace. Thus the resistor on surface of substrate is connected to the circuit trace through contact 16) through said first opening (16)., and wherein said circuit trace comprises a third metal layer (copper, tungsten, nicket col 6 lines 55-57) and a copper layer (electroplating copper, col 6 lines 57) over said third metal layer.

Lin fails to disclose the resistor in said silicon substrate comprises silicon with a dopant. Woolery teaches a chip structure (Figures 4A-4J) with a silicon substrate (400) and a resistor (“Resistor”) in said silicon substrate, where said resistor comprises silicon

with a dopant (arsenic, col 9 lines 53-56). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lin to have a resistor in the silicon substrate where said resistor comprises silicon with a dopant as in Woolrey in order to be able to predetermine and set the device resistivity.

Re claims 48-53 and 94-99: Lin discloses a polymer layer (20) on the passivation layer (18) and the circuit trace (26/22/21/36/28) and wherein said circuit trace is further on the polymer layer and the polymer layer comprises polyimide (PI) or benzocyclobutene (BCB), (col 5, lines 19 and 23-27).

Claims 54-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,495,442 to Lin et al (Lin) in view of U.S. Pat. No. 6,528,380 to Woolery et al. (Woolery) and U.S. Pat. No. 6,235,101 to Erdejac et al. (Erdejac).

Re claims 54-58: Lin discloses the circuit structure as claimed in 43. Lin fails to explicitly disclose the structure comprising an inductor over said passivation layer where said inductor comprises a copper layer. Erdejac teaches an inductor (top metal inductor Fig 20c) over said passivation layer where said inductor comprises: a copper layer (col 6 lines 65-68); a gold layer (col 7 line 25-26); or a titanium-tungsten alloy layer and a copper layer over said titanium-tungsten alloy layer (col 6 lines 57-60). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lin to have the inductor as in Erdejac in order to create a circuit structure for specific applications such as RF.

Re claim 59: Lin discloses the circuit structure as claimed in 43. Lin fails to explicitly disclose the structure comprising a capacitor over said silicon substrate. Erdejac teaches a capacitor (Fig 20b, poly poly capacitor) over said silicon substrate, a second dielectric layer (between poly 0 and poly 1) on said first electrode (poly 0) and in the third opening, a second electrode (poly 1) on said second dielectric layer and over aid first electrode. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lin to include the capacitor as in Erdejac in order to create a circuit structure for specific applications such as RF.

Claims 64, 60-63, 69-74, 83-84 and 100-102 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,495,442 to Lin et al (Lin) in view of U.S. Pat. No. 6,528,380 to Woolery et al. (Woolery) and U.S. Pat. No. 6,486,530 to Sasagawa et al. (Sasagawa) or U.S. Pat. No. 6,495,442 to Lin et al (Lin) in view of U.S. Pat. No. 6,528,380 to Woolery et al. (Woolery) and U.S. Pat. No. 6,235,101 to Erdejac et al. (Erdejac) and U.S. Pat. No. 6,486,530 to Sasagawa et al. (Sasagawa).

Re claim 64: Lin discloses a chip structure comprising:

a silicon substrate (10, col 4 line 49);

a resistor in said silicon substrate (not shown but "transistors and other devices" is described in col 4 lines 49-51),

a MOS device (not shown but described as "transistors and other devices" in col 4 lines 49-51) comprising a portion in said silicon substrate;

a metallization structure (14) over said silicon substrate, wherein said metallization structure comprises a first metal layer (interconnect portion 13 of first layer of 14) and a second metal layer (interconnect portion 13 of second layer of 14) over said first metal layer;

a dielectric (white portion of layer 14) layer between said first and second metal layers;

a passivation layer (18, col 5 lines 4-5) over the metallization structure and over said dielectric layer, herein a first opening in said passivation layer is over a first contact point (16; col 4 lines 57-67) of said metallization structure and said first contact point is at a bottom of said first opening, and wherein a second opening (16) in said passivation layer is over a second contact point of said metallization structure and said second contact point is at a bottom of said second opening, wherein a gap (created by passivation layer 18) is between said first and second contact points, wherein said passivation layer comprises an insulating nitride layer (col 5 lines 4-5); and

a circuit trace (26/22/36/28/38) over the passivation layer and on said first and second contact points (16), wherein said first contact point is connected to said second contact point through said circuit trace (38/28/38 connect first and second points 16), wherein said circuit trace is connected to said resistor (col 4 lines 66-67, col 5 line 1-2 describe point of contact 16 as connected to the transistors and other devices on the surface of substrate 10, which would include the resistor. col 5 lines describe contact point 16 also in electrical contact with 22/36/38, which is the circuit trace. Thus the

resistor on surface of substrate is connected to the circuit trace through contact 16) through said first opening (16).

Lin fails to disclose the resistor in said silicon substrate comprises silicon with a dopant. Woolery teaches a chip structure (Figures 4A-4J) with a silicon substrate (400) and a resistor ("Resistor") in said silicon substrate, where said resistor comprises silicon with a dopant (arsenic, col 9 lines 53-56). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lin to have a resistor in the silicon substrate where said resistor comprises silicon with a dopant as in Woolrey in order to be able to predetermine and set the device resistivity.

Lin also fails to disclose where said circuit trace comprises a titanium-containing layer and a gold layer over said titanium-containing layer. Sasagawa teaches a circuit trace (109-111) comprises a titanium-containing layer (109, col 4 line 14) and a gold layer (111, col 4 line 21) over said titanium-containing layer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lin to include the different circuit trace and metallization layers of Sasagawa in order to optimize the device performance under thermal stress.

Re claims 60-63, 83-84 and 100-102: Lin as modified discloses the device of 43, 65 and 89 as above where the circuit trace comprises a nickel layer over a copper layer. Lin fails to disclose the circuit trace comprising aluminum or a gold layer over the copper layer, a titanium layer under the copper layer, a titanium-containing layer comprising tungsten, a chromium layer under the copper layer, a gold layer, a titanium-containing layer under gold layer and a titanium-containing layer comprising tungsten. a

Sasagawa teaches a circuit trace/capacitor second electrode (109-111) comprises aluminum, or nickel layer over a copper layer and the circuit trace comprising a gold layer over the copper layer, a titanium layer under the copper layer, a chromium layer under the copper layer, a gold layer, a titanium-containing layer under gold layer and a titanium-containing layer (col 4 lines 13-22). Erdejac teaches a titanium-containing layer comprising a titanium-tungsten alloy (col 6 lines 57-60).. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lin to include the different circuit trace and metallization layers of Sasagawa and Erdejac in order to optimize the device performance under thermal stress.

Re claims 69-74: Lin discloses a polymer layer (20) between the passivation/silicon-nitride layer (18) and the circuit trace (26/22/21/36/28) and on the circuit trace where the polymer layer comprises polyimide (PI) or benzocyclobutene (BCB), (col 5, lines 19 and 23-27).

Claims 44-46, 65-67, 90-92 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,495,442 to Lin et al (Lin) in view of U.S. Pat. No. 6,528,380 to Woolery et al. (Woolery) as applied to claims 44 and 89 above and U.S. Pat. No. 6,495,442 to Lin et al (Lin) in view of U.S. Pat. No. 6,528,380 to Woolery et al. (Woolery) and U.S. Pat. No. 6,486,530 to Sasagawa et al. (Sasagawa) as applied to claim 64 above and in further view of U.S. Pub. No. 2003/0155570 to Leidy.

Re claims 44-46, 65-67, 90-92, Lin as modified discloses the device of 43, 65, and 89 as above. The modification of Woolery also discloses the resistor comprising

silicon with a dopant of arsenic (col 9 lines 51 line 6). Lin as modified fails to disclose the resistor comprising silicon with a dopant of boron, phosphorous. Leidy teaches a resistor comprising silicon and a dopant of boron, phosphorous, or arsenic (page 5, claim 26). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lin to have the resistor made of silicon and a dopant of boron, phosphorous, or arsenic as in Leidy in order to be able to predetermine the device resistivity (Leidy, page 3, paragraph 37).

Claims 45, 47, 66, 68, 91 and 93 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,495,442 to Lin et al (Lin) in view of U.S. Pat. No. 6,528,380 to Woolery et al. (Woolery) as applied to claims 43 and 89 above and U.S. Pat. No. 6,495,442 to Lin et al (Lin) in view of U.S. Pat. No. 6,528,380 to Woolery et al. (Woolery) and U.S. Pat. No. 6,486,530 to Sasagawa et al. (Sasagawa) as applied to claim 64 above in further view of and U.S. Pub. No. 2003/0183332 to Simila.

Re claims 45, 47, 66, 68, 91 and 93: Lin as modified discloses the device of 43, 65 and 89 as above. The modification of Woolery also discloses the resistor comprising silicon with a dopant of arsenic (col 9 lines 51 line 6). Lin as modified fails to disclose the resistor comprising silicon with a dopant of phosphorous or gallium. Simila a resistor comprising silicon and a dopant of phosphorous or gallium (paragraph 70). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lin to have the resistor made of silicon and a dopant of phosphorous or gallium as in Simila in order to be able to predetermine the device resistivity.

Response to Arguments

Applicant's arguments filed 08/24/2009 have been fully considered but they are not persuasive.

Applicant argues (Remarks, page 12, 14-15, and 17-18) that the Examiner's interpretation of Lin's disclosure of "transistors and other devices" in the silicon substrate to include resistors is improper because Lin exact description does not include "a resistor in a silicon substrate." The Examiner notes that while Lin does not explicitly disclose resistors, the state of the art at the time of the invention provides sufficient evidence to conclude that Lin's disclosure encompasses resistors in the silicon substrate as well. The Examiner maintains that one of ordinary skill in the art at the time the invention was made would interpret "transistors and other devices" to include resistors; as transistor and resistors are known semiconductor devices that are commonly placed in substrates. This is further supported by many references, including the secondary reference Woolery which discloses a silicon substrate with transistors (440) and resistors (420) see Fig 4E. Additionally other references disclosing metallization also disclose transistors and resistors within a substrate, for example U.S. Pat. No. 6,261,944 to Mehta et al. (col 3 lines 45-57) and U.S. Pat. No. 5,328,553 to Poon (col 5 lines 33-38).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Colleen A. Matthews whose telephone number is

(571)272-1667. The examiner can normally be reached on Monday - Friday 8AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/C. A. M./
Examiner, Art Unit 2811

/Lynne A. Gurley/
Supervisory Patent Examiner, Art Unit 2811